AMENDMENTS TO THE CLAIMS

Please replace all prior versions of the claims with the following claim listing:

Claims:

1-22. (Canceled)

23. (New) A method for testing an integrated circuit, the method comprising:

defining a list of faults for which an integrated circuit is tested;

generating a test vector comprising a plurality of bits defining test inputs to the integrated circuit;

assigning values to a portion of the plurality of bits of the test vector to detect at least one unmarked target fault selected from the list of faults, whereby a remainder of the bits of the test vector are left as unspecified bits;

marking said at least one unmarked target fault as detected;

repeating the generating, assigning, and marking until all target faults of the list of faults are marked;

non-randomly filling a plurality of the unspecified bits for each test vector with values that enable each test vector to be compressed; and

compressing each test vector to create a compressed vector having fewer bits.

24. (New) The method of claim 23, wherein the unspecified bits are non-randomly filled after all target faults are marked.

25. (New) The method of claim 23, wherein non-randomly filling the plurality of the unspecified bits further comprises filling each of the plurality of the unspecified bits to a value of zero.

26. (New) The method of claim 23, wherein non-randomly filling the plurality of the unspecified bits further comprises filling each of the plurality of the unspecified bits to a value of one.

27. (New) The method of claim 23, wherein non-randomly filling the plurality of the unspecified bits further comprises filling subsequent unspecified bits with the value of a latest specified bit.

28. (New) The method of claim 23, wherein non-randomly filling the plurality of the unspecified bits further comprises filling each of the plurality of the unspecified bits with a repeating pattern of ones and zeros.

29. (New) The method of claim 23, further comprising randomly filling a second plurality of unspecified bits for each test vector.

30. (New) The method of claim 23, wherein said repeating the generating further comprises:

determining whether a currently generated test vector may be compacted with a previously generated test vector, and if so, compacting the currently generated test vector with the previously generated test vector, and if not, adding the currently generated test vector to a set of test vectors.

31. (New) The method of claim 30, wherein said determining is performed before said non-randomly filling.

32. (New) The method of claim 30, wherein said determining is performed during said non-randomly filling.

33. (New) The method of claim 30, wherein said determining is performed after said non-randomly filling.

34. (New) The method of claim 23, wherein the assigning further comprises assigning values to only those bits of the test vector for detecting a single unmarked target fault selected from the list of faults.

35. (New) The method of claim 23, further comprising:

fault simulating a generated test vector to determine if the test vector detects additional faults, and if so, marking said additional faults as detected.

36. (New) An apparatus for generating a set of test vectors, the apparatus comprising:

means for evaluating a list of faults for which an integrated circuit is tested;

means for generating a first test vector comprising a plurality of bits defining test inputs to the integrated circuit;

means for assigning values to a fraction of the plurality of bits of the first test vector to detect at least one target fault selected from the list of faults, whereby a remainder of the bits of the first test vector are left as unspecified bits;

means for marking the at least one target fault as detected;

wherein the means for generating further generates another test vector comprising a plurality of bits defining test inputs to the integrated circuit;

wherein the means for assigning further assigns values to a fraction of the plurality of bits of said another test vector until all target faults are detected, the values being assigned to detect at least one unmarked target fault selected from the list of faults, whereby a remainder of the bits of said another test vector are left as unspecified bits;

wherein the means for marking further marks said at least one unmarked target fault as detected until all target faults of the list of faults are marked;

means for non-randomly filling a plurality of the unspecified bits for each test vector with values that enable each test vector to be compressed; and

means for compressing each test vector to create a compressed vector having fewer bits.

37. (New) The apparatus of claim 36, wherein the means for non-randomly filling fills the plurality of unspecified bits after all target faults are marked.

38. (New) The apparatus of claim 36, wherein the means for non-randomly filling the plurality of the unspecified bits further comprises means for filling each of the plurality of the unspecified bits to a value of zero.

39. (New) The apparatus of claim 36, wherein the means for non-randomly filling the plurality of the unspecified bits further comprises means for filling each of the plurality of the unspecified bits to a value of one.

40. (New) The apparatus of claim 36, wherein the means for non-randomly filling the plurality of the unspecified bits further comprises means for filling subsequent unspecified bits with the value of a latest specified bit.

41. (New) An automatic test pattern generator (ATPG) for testing an integrated circuit for a list of faults, the ATPG comprising:

logic for generating a set of test vectors, each test vector of the set of test vectors containing a plurality of bits defining test inputs to the integrated circuit;

logic for assigning values to a number of bits for each test vector such that each test vector is capable of detecting at least one target fault selected from the list of faults, whereby a remainder of the bits of each test vector are left as unspecified bit positions, the logic for assigning continuing to assign values to the bits of the test vectors until all target faults in the list of faults are detected; and

logic for non-randomly filling a plurality of the unspecified bit positions for each test vector after the logic for assigning has assigned values to detect all target faults, the logic for non-randomly filling thereby enabling each test vector to be compressed; and

logic for compressing each test vector to create a compressed vector having fewer bits.

42. (New) The ATPG of claim 41, wherein the logic for non-randomly filling the plurality of unspecified bit positions is further configured to randomly fill a second plurality of unspecified bit positions for each test vector.

43. (New) The ATPG of claim 41, further comprising:

logic for compacting the set of test vectors to the fullest possible extent.

44. (New) The ATPG of claim 43, wherein the logic for compacting performs compaction before the logic for non-randomly filling performs filling the unspecified bit positions.